

LH534000B-S

CMOS 4M (512K × 8/256K × 16)
3V-Drive Mask-Programmable ROM

FEATURES

- 524,288 words × 8 bit organization (Byte mode)
262,144 words × 16 bit organization (Word mode)
- Access times:
 - 500 ns ($2.6\text{ V} \leq V_{CC} < 4.5\text{ V}$)
 - 200 ns ($4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$)
- Wide range power supply: 2.6 to 5.5 V
- Static operation
- Three-state outputs
- Packages:
 - 40-pin, 600-mil DIP
 - 40-pin, 525-mil SOP
 - 48-pin, $12 \times 18\text{ mm}^2$ TSOP (Type I)

DESCRIPTION

The LH534000B-S is a 4M-bit mask-programmable ROM organized as $524,288 \times 8$ bits (Byte mode) or $262,144 \times 16$ bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

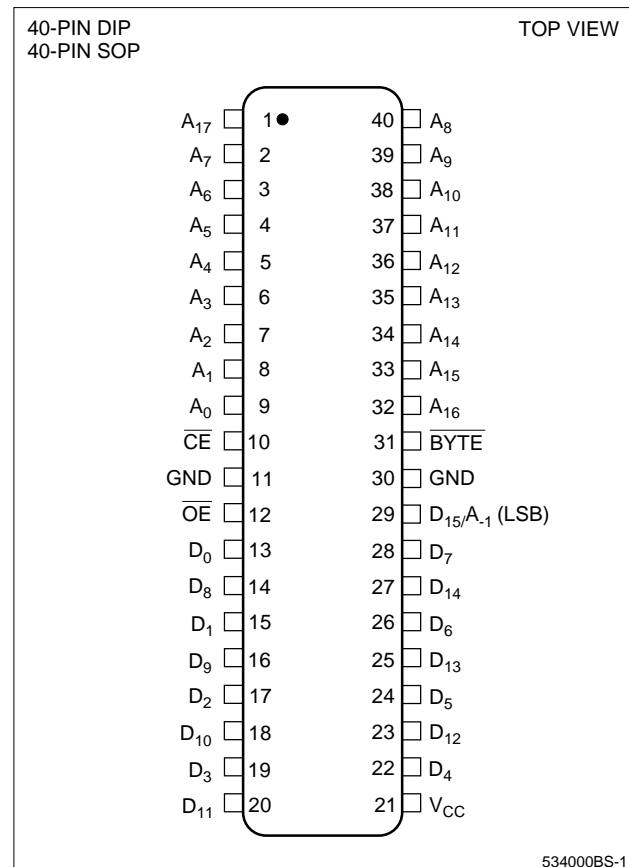


Figure 1. Pin Connections for DIP and SOP Packages

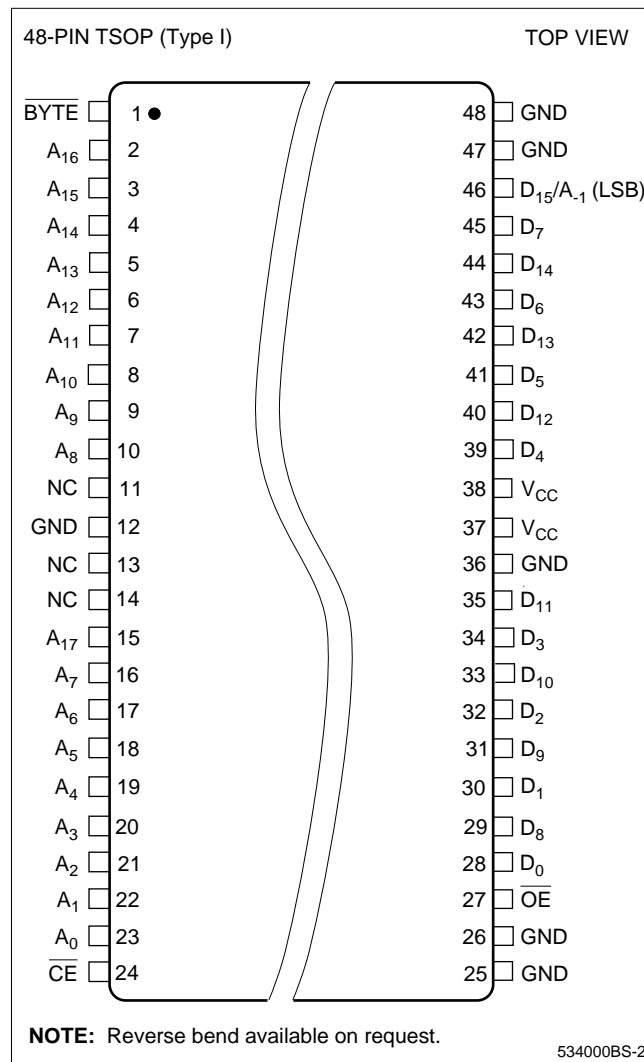


Figure 2. Pin Connections for TSOP Package

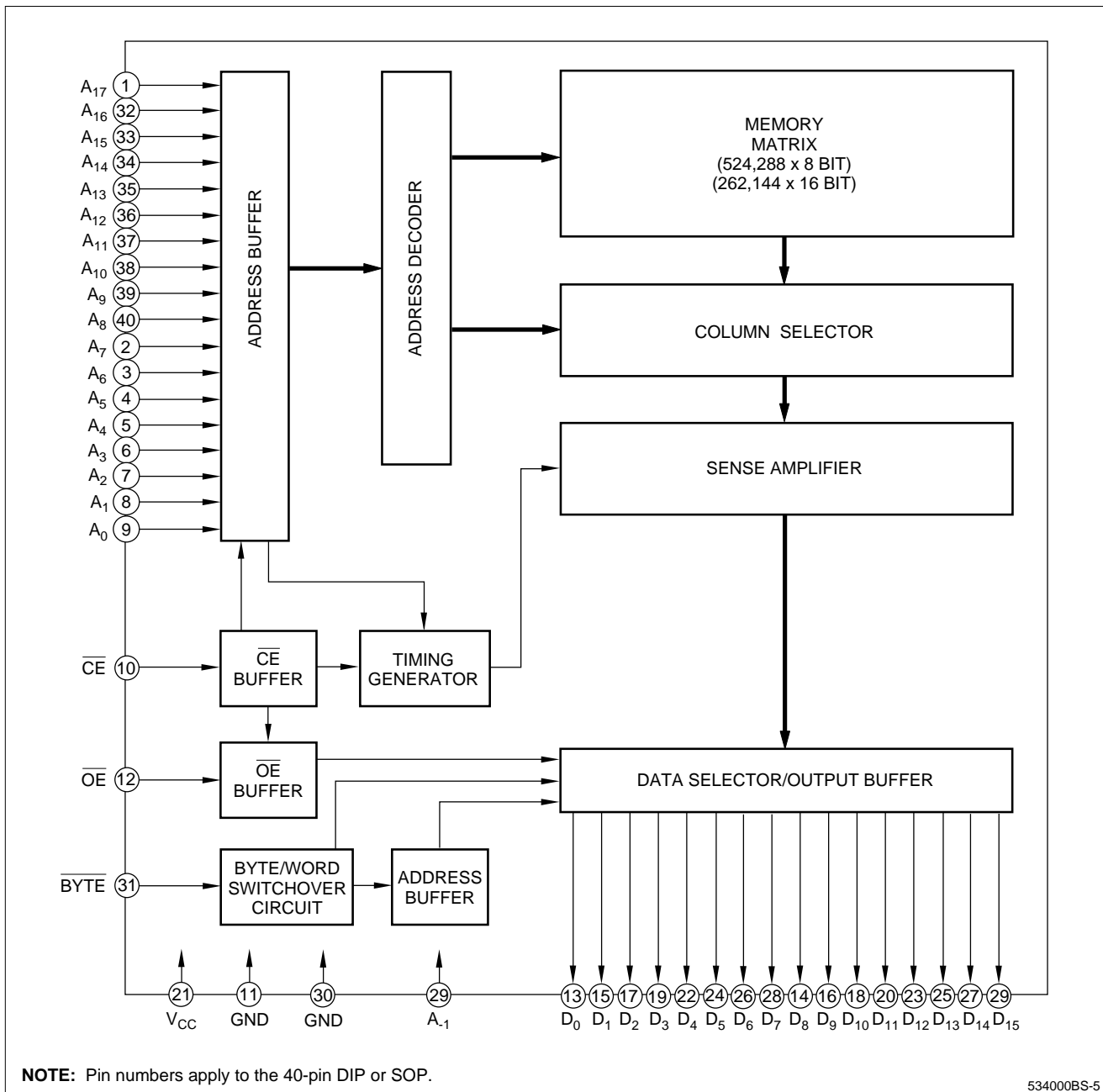


Figure 3. LH534000B-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₋₁ – A ₁₇	Address input	1
D ₀ – D ₁₅	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE	Output enable input	
V _{CC}	Power supply	
GND	Ground	

NOTE:

- The D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the bit configuration is set to byte mode, and data output (D₁₅) when in word mode. The BYTE input pin selects bit configuration.

TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{BYTE}	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
			D ₀ – D ₇	D ₈ – D ₁₅	LSB	MSB	
H	X	X	High-Z	High-Z	–	–	Standby
L	H	X	High-Z	High-Z	–	–	Operating
L	L	H	D ₀ – D ₇	D ₈ – D ₁₅	A ₀	A ₁₇	Operating
L	L	L	D ₀ – D ₇	High-Z	A ₋₁	A ₁₇	Operating

NOTE:

X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	–0.3 to +7.0	V
Input voltage	V _{IN}	–0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	–0.3 to V _{CC} + 0.3	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}		0.8 V _{CC}	V _{CC} + 0.3	V	
Input 'Low' voltage	V _{IL}		–0.3	0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = –100 μA	0.8 V _{CC}		V	
Output 'Low' voltage	V _{OL}	I _{OL} = 400 μA		0.4	V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}		10	μA	1
Operating current	I _{CC1}	t _{RC} = 200 ns		50	mA	2
	I _{CC2}	t _{RC} = 1 μs		45	mA	2
	I _{CC3}	t _{RC} = 200 ns		45	mA	3
	I _{CC4}	t _{RC} = 1 μs		40	mA	3
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$		100	μA	
Input capacitance	C _{IN}	f = 1 MHz		10	pF	
Output capacitance	C _{OUT}	T _A = 25°C		10	pF	

NOTES:

1. $\overline{CE}/\overline{OE} = V_{IH}$
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE} = V_{IL}$, outputs open
3. V_{IN} = (V_{CC} – 0.2 V) or 0.2 V, $\overline{CE} = 0.2 V$, outputs open

AC CHARACTERISTICS ($T_A = 0$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	$2.6 \leq V_{CC} < 4.5$		$4.5 \leq V_{CC} \leq 5.5$		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		200		ns	
Address access time	t_{AA}		500		200	ns	
Chip enable access time	t_{ACE}		500		200	ns	
Output enable delay time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		10		ns	
CE to output in High-Z	t_{CHZ}		150		80	ns	1
OE to output in High-Z	t_{OHZ}		150		80	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to 0.8 V_{CC}
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF

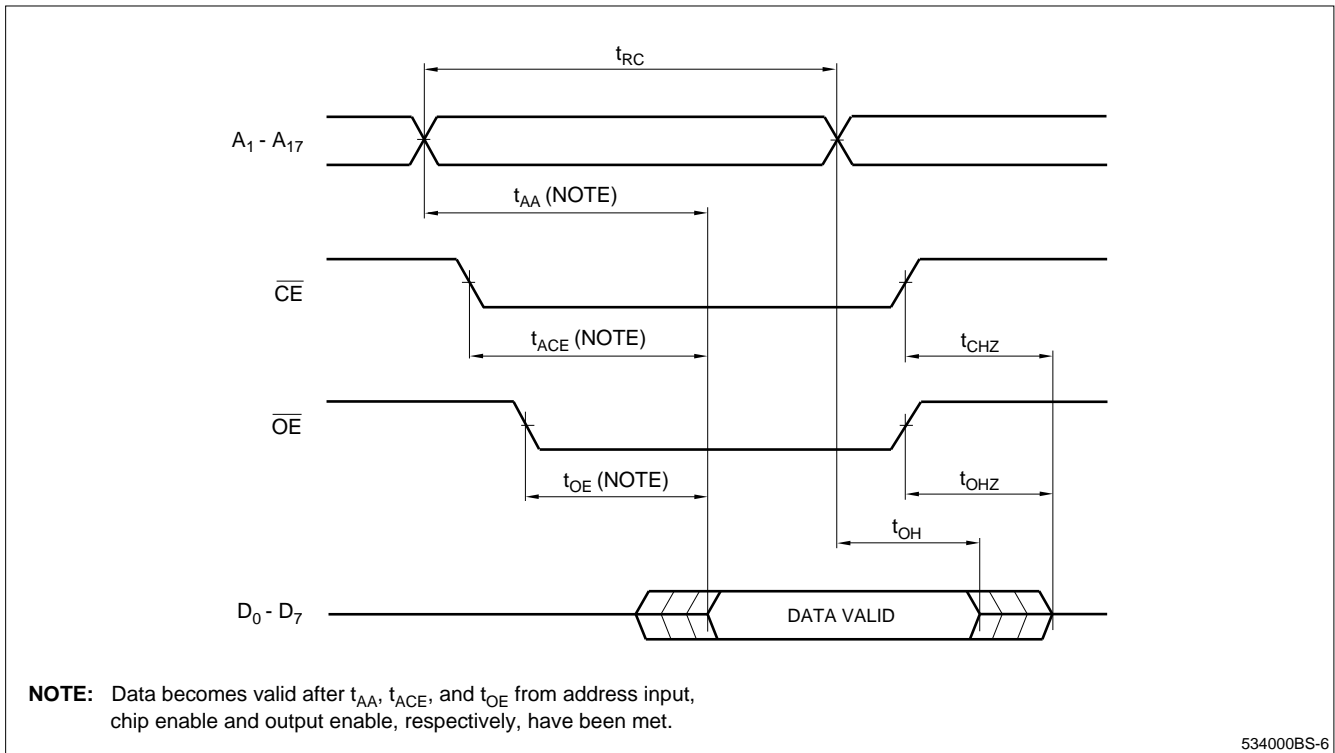


Figure 4. Byte Mode ($\overline{BYTE} = V_{IL}$)

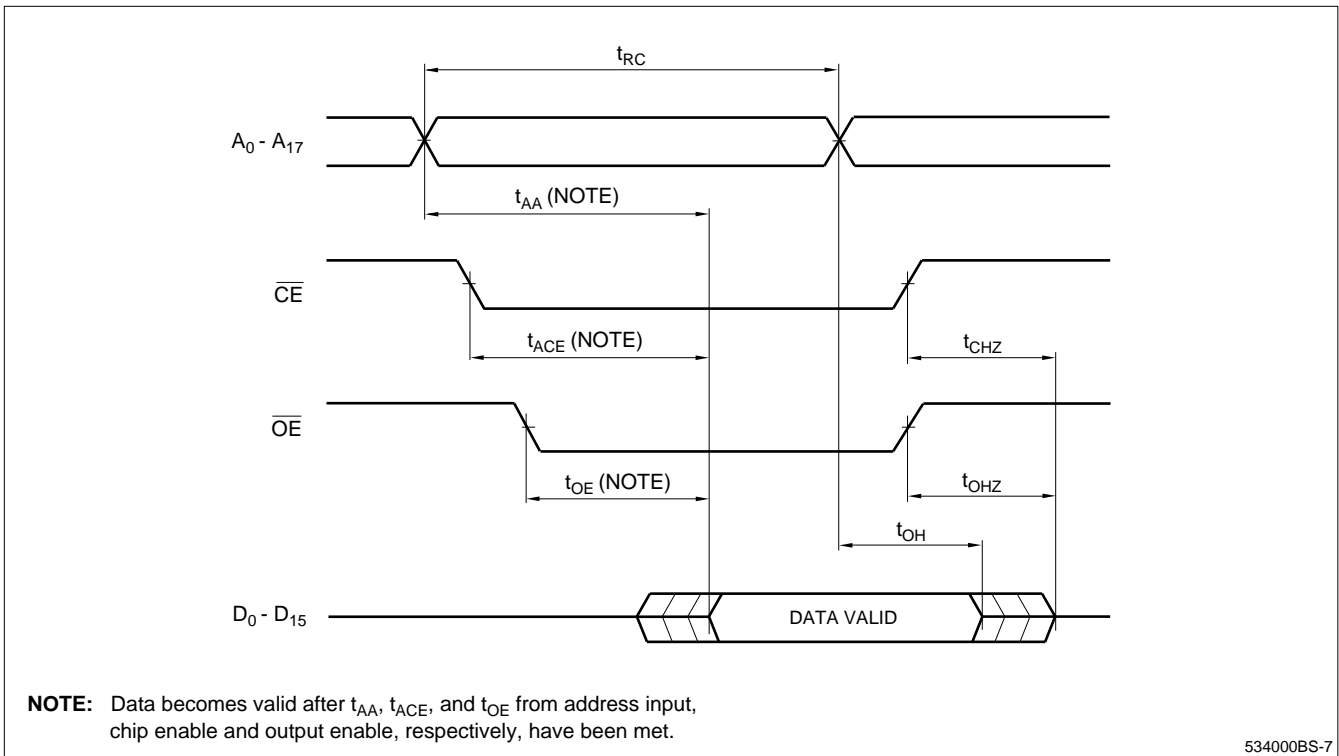
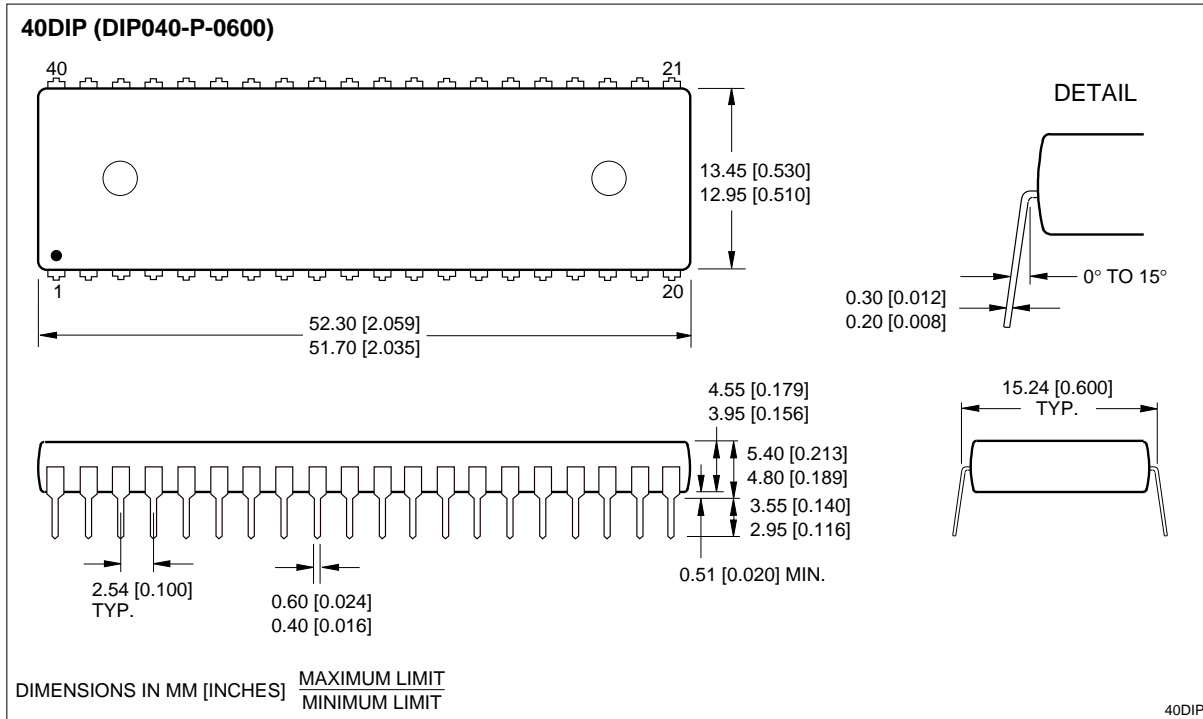
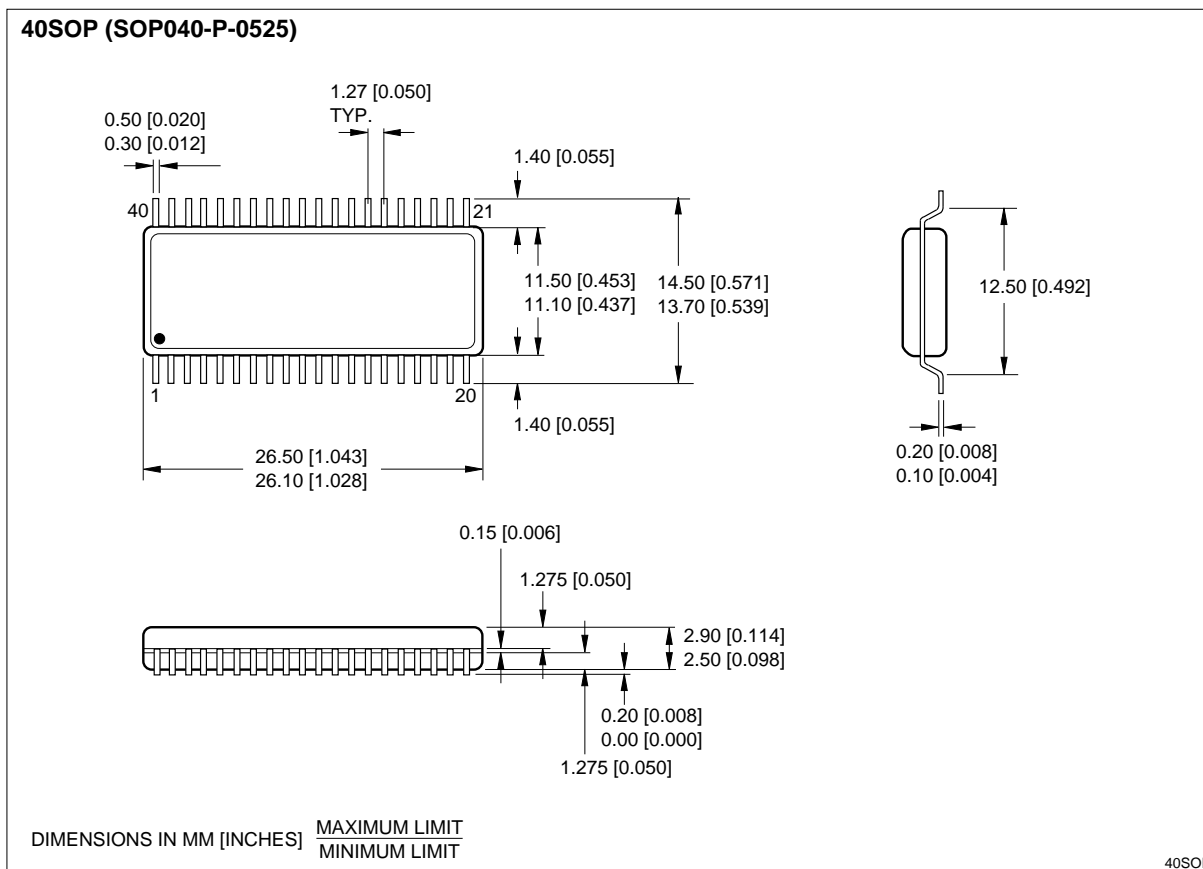


Figure 5. Word Mode ($\overline{BYTE} = V_{IH}$)

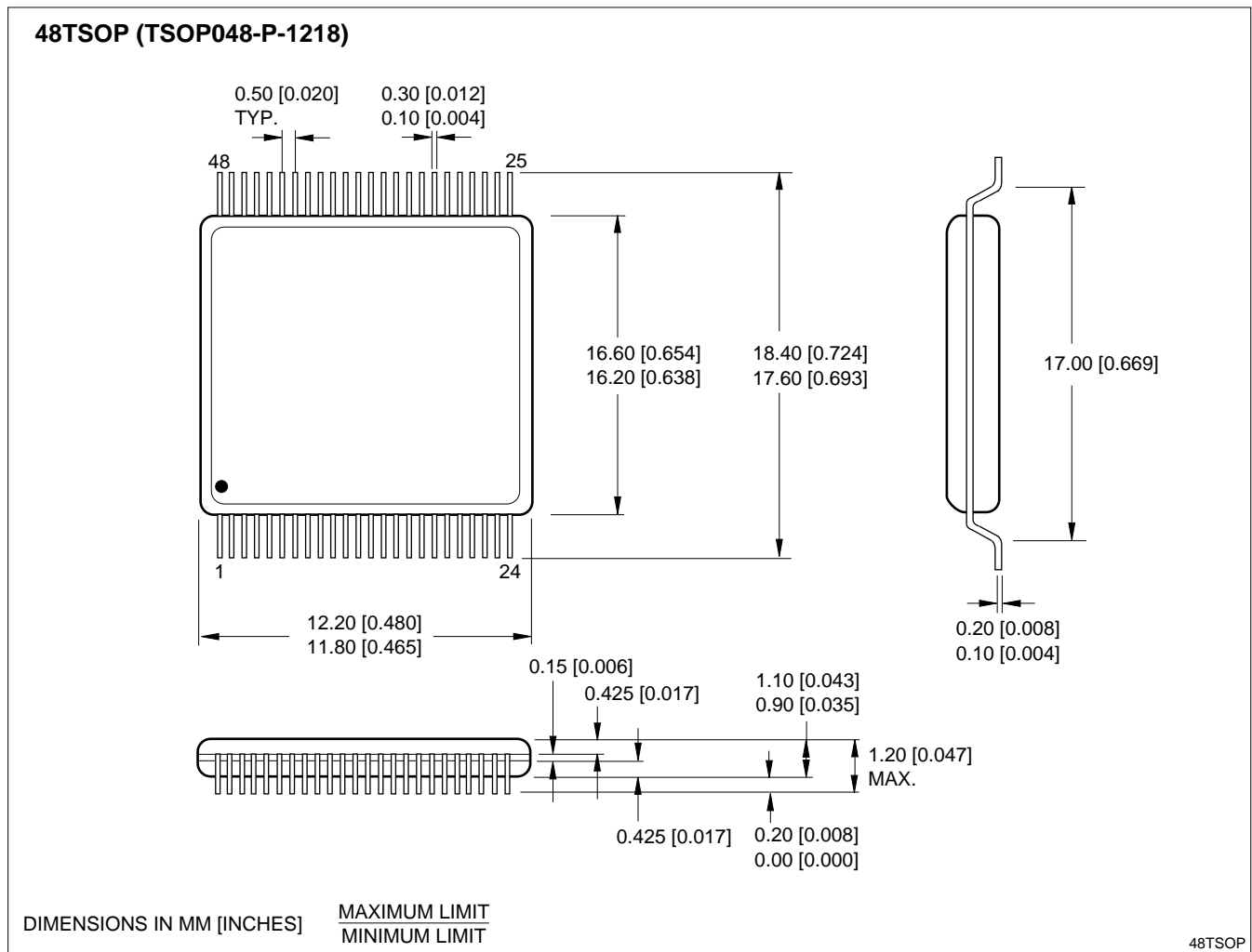
PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP



48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION

LH534000B	X	- S
Device Type	Package	Low-Voltage Operation
		D 40-pin, 600-mil DIP (DIP040-P-0600)
		N 40-pin, 525-mil SOP (SOP040-P-0525)
		T 48-pin, 12 x 18 mm ² TSOP (Type I) (TSOP048-P-1218)
		TR 48-pin, 12 x 18 mm ² TSOP (Type I) Reverse bend (TSOP048-P-1218)
	CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM	
Example: LH534000BD-S (CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM, Low-Voltage Operation, 40-pin, 600-mil DIP)		

534000BS-8